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DESIGN OF EFFICIENT SHIFT REGISTERS USING PULSED LATCHES

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Abstract:

This paper proposes a low-power and area-efficient shift register using digital pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register using pulsed latches was fabricated using a 0.18μm CMOS process with VDD = 1.8V. The core area is 6600μm2. The power consumption is 1.2mW at a 100 MHz clock frequency.

Keywords: Area-efficient, flip-flop, pulsed clock, pulsed latch, shift register.

1. INTRODUCTION

Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers of transistors onto the same die. Heat is one of the phenomenon packaging challenges in this epoch, it is one of the main challenges of low power design methodologies and practices. Another driver of low power research is the reliability of the integrated circuit. More switching implies higher average current is expelled and therefore the probability of reliability issues occurring rises. We are moving from laptops to tablets and even smaller computing digital systems. With this profound trend continuing and without a match trending in battery life expectancy, the more low power issues will have to be addressed. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today's and future integrated chips. Power] consumption of Very Large Scale Integrated design is given by Generalized relation, P = CV2f [1].

Since power is proportional to the square of the voltage as per the relation, voltage scaling is the most prominent way to reduce power dissipation. However, voltage scaling is results in threshold voltage scaling which bows to the exponential increase in leakage power. Though several contributions have been made to the art of single edge triggered flip-flops, a need evidently occurs for a design that further improves the performance of single edge triggered flipflops patterns. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flipflop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shiftregister to reduce the area and power consumption.

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2. SHIFT REGISTERS

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers and image processing ICs Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register A 16- megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations.The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flipflops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

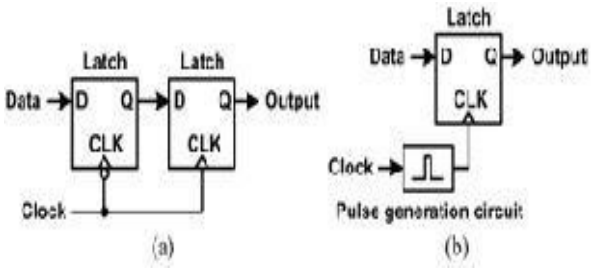

Fig.1. (a) Master slave flip flop (b) Pulsed latch

There are also 'bidirectional' shift registers which allow shifting in both directions:L→R or R→L. The serial input and last output of a shift register can also be connected to shift register' Previous work often measured energy consumption using a limited set of data patterns with the clock switching every cycle. But real designs have a wide variation in clock and data activity across different TE instances. For example, lowpower microprocessors make extensive use of clock gating resulting in many TEs whose energy consumption is dominated by input data transitions rather than clock transitions.

3. PROPOSED ARCHITECTURE

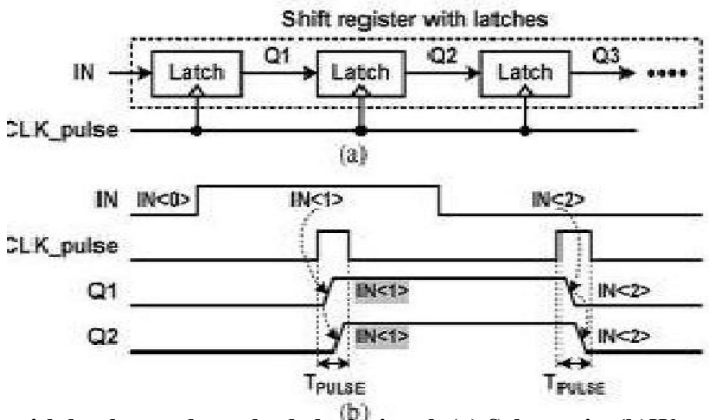

Fig. 2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b)Waveforms

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The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift registers in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant during the clock pulse width (TPULSE). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. One solution for the timing problem is to add delay circuits between

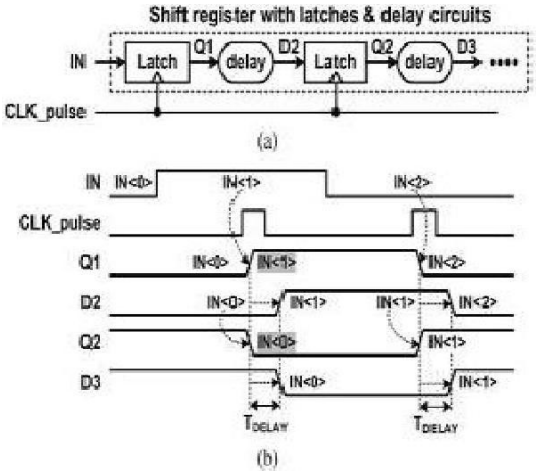

Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a)Schematic. (b)Waveforms

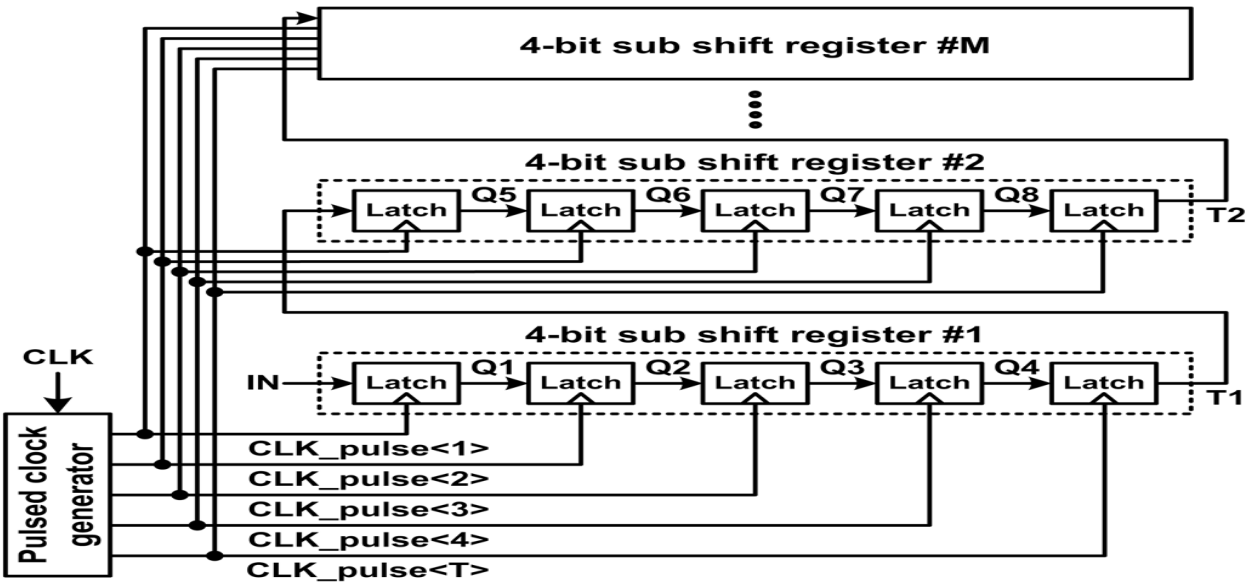

Fig.4 . Proposed Shift register

latche. The output signal of the latch is delayed and reaches the next latch after the clock pulse. the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant

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input signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power over heads.The proposed shift register is divided into M sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bitsub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals(CLK_pulse1:4 and CLK _pulseT). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2.

4. RESULTS

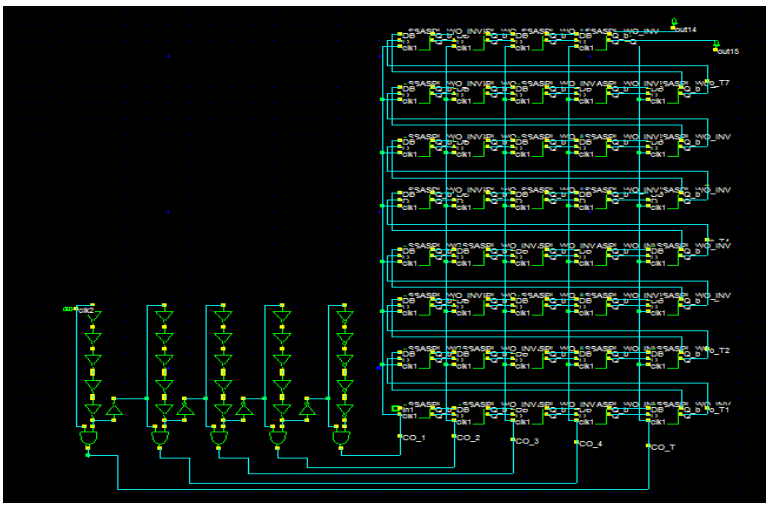

Fig:5. 32 Bit Shift Register using SSASPL

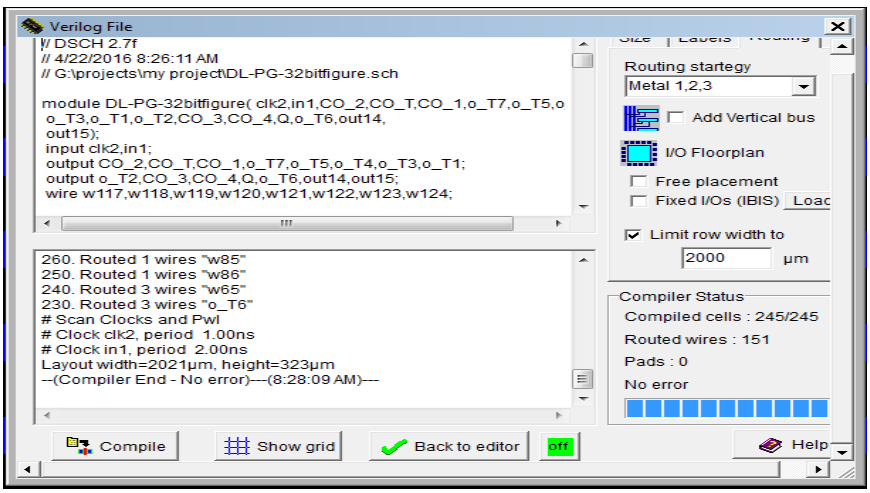

Fig:6 Area of the 32 Bit Shift Register using SSASPL

The proposed shift register using pulsed latches were implemented with the 32 and 16 bit SSASPLs achieves a small area and low power consumption compared to the 32 and 16 bit PPCFF.

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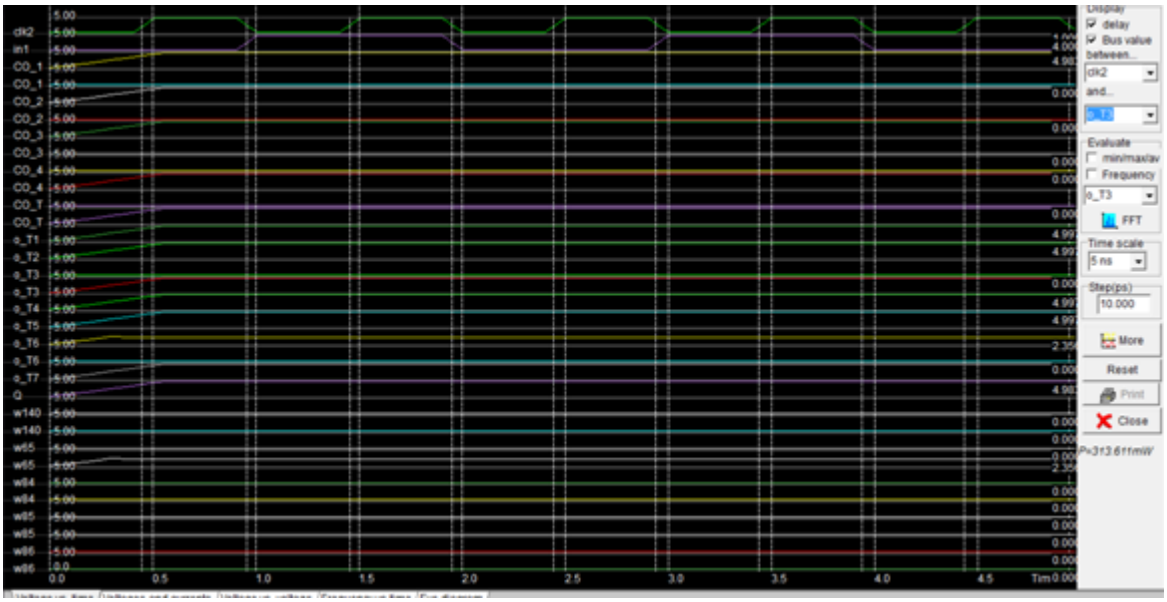

Fig:7 Power of the 32 Bit Shift Register using SSASPL

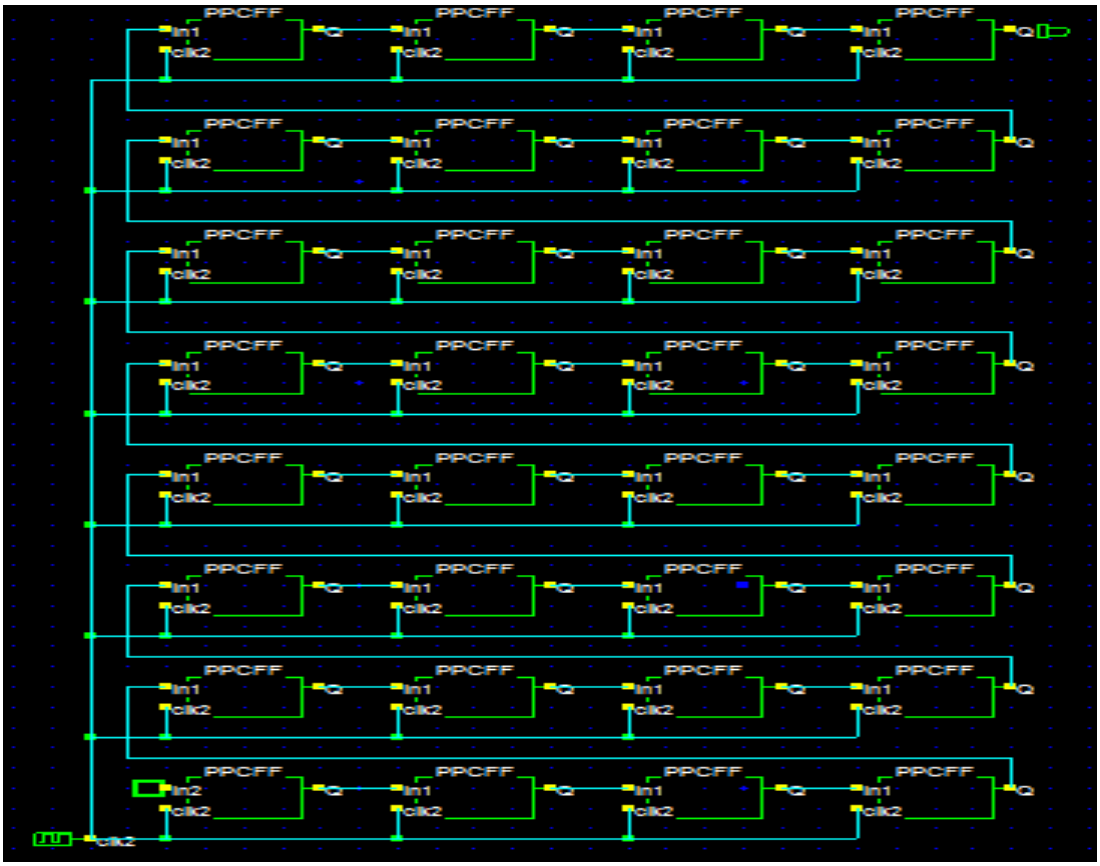

Fig:8. 32 Bit Shift Register using PPCFF

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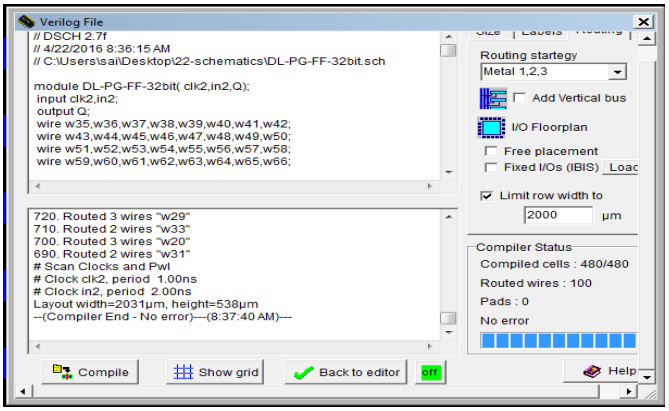

Fig:9. Area of the 32 Bit Shift Register using PPCFF

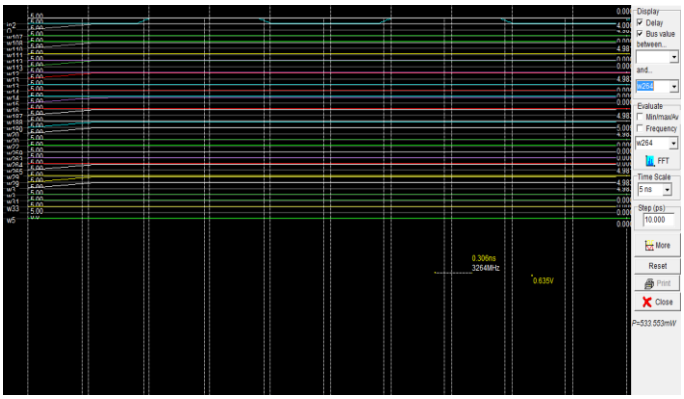

Fig:10 : Power of the 32 Bit Shift Register using PPCFF

COMPARISION ANALYSIS

PARAMETERS	PPCFF	SSASPL
1. Area	31.41μm^2	8.42μm^2
2. Power	6.611 [mW]	2.876 [mW]

Table:1 Comparision of Area and Power of SSASPL and PPCFF

PARAMETERS	PPCFF	SSASPL
1. Area	60.25 μm^2	33.63μm^2
2. Power	244.92 [mW]	381.39 [mW]

Table:2 Comparision of Area and Power of 16 bit Shift Register using SSASPL and PPCFF

PARAMETERS	PPCFF	SSASPL
1. Area	90.926 μm^2	6.527 μm^2
2. Power	533.55 [mW]	313.61 [mW]

Table:3 Comparision of Area and Power of 32 bit Shift Register using SSASPL and PPCFF

CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by substituting flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals as an alternative of a single pulsed clock signal.

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