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ENERGY EFFICIENT FREQUENCY MULTIPLIER FOR SILICON ON CHIP

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Abstract:

A logic gate-based digital frequency multiplication technique for low-power frequency synthesis is presented. The proposed digital edge combining approach offers broadband operation with low- power and low-area advantages and is a promising candidate for low- power frequency synthesis in deep submicrometer CMOS technologies. Chip prototype of the proposed frequency multiplication-based 2.4-GHz binary frequency-shift-keying (BFSK)/amplitude shift keying (ASK) transmitter (TX) was fabricated in 0.13-µm CMOS technology. The TX achieves maximum data rates for BFSK and ASK modulations, respectively, consuming The corresponding energy efficiencies for BFSK for ASK modulations.

Key words: Binary frequency-shift-keying (BFSK) transmitter (TX), class-D power amplifier (PA), energy efficient, frequency multiplication technique.

1. INTRODUCTION

Low-power and low-area transmitter (TX) architectures are essen- tial for short-range communications such as wireless sensor networks, body area networks, and other battery operated applications. These low-power applications have relaxed requirements on phase noise, spectral purity, and other performance metrics of TX, which can be used as an extra degree of freedom in the TX architecture design. Phase-locked loop (PLL)-based TXs are both power and area efficient compared with the conventional mixer-based direct up-conversion TX architectures.

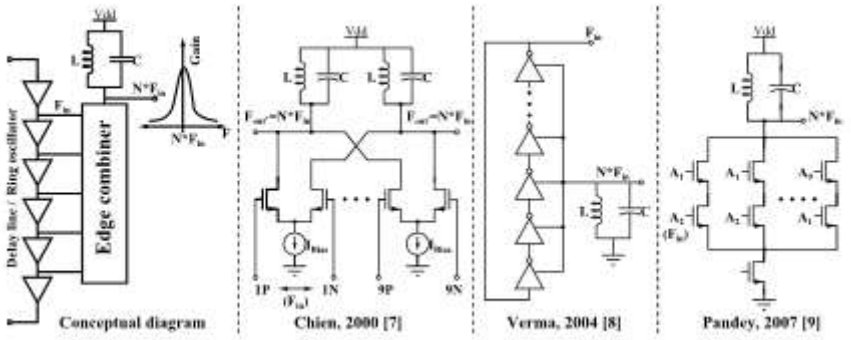

Fig.1. Frequency multiplication circuit techniques

The power consumption in frequency synthesis can be minimized by operating the PLL at lower frequencies and using frequency multiplier circuits outside the loop to generate the up-converted RF carrier The power consumption in frequency synthesis can be minimized by operating the PLL at lower frequencies and using frequency multiplier circuits outside the loop to generate the up-

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converted RF carrier, Open-loop PLL-based TX achieves high data rates, but its trans- mission quality is affected by the increased close-in phase noise of voltage-controlled oscillator (VCO), frequency drift due to pressure, volume, and temperature (PVT) variations and disturbances in VCO control line during modulation, and other nonideal effects. In this brief, we exploit the higher transition frequency (90 GHz, 130 nm) and improved matching performance (for the same device area, W*L) [11] offered by the deep submicrometer devices and demonstrate a static logic gate-based frequency multiplier design for low-power frequency synthesis. The presented digital edge combiner (EC) offers broadband operation with rail-to-rail output swing, low-power, and low-area implementation advantages. The power and area advantages of the proposed digital frequency mul- tiplier comes with a tradeoff in the spectral purity of the generated RF carrier, which is acceptable in the low-power and short-range wireless communication standards.

2. FREQUENCY MULTIPLICATION

The block diagram of frequency multiplication-based binary frequency-shift-keying (BFSK)/amplitude shift keying a small area penalty. As only one PD-N is added to each differential output of the edge combiner when the maximum multiplication ratio is increased by one, the output loading of the edge combiner increases slower than that of the edge combiner in . However, the PD-N should remain on till the positive and the negative edges of the multiplied differential clocks are generated by the edge combiner. In addition, when the PD-N is turned ON, the edge combiner uses a small-sized PU-P to prevent conflict between the PU-P and the PD-N. Because of these restrictions, the frequency multiplier in may not be suitable for high-speed operation and cannot guarantee 50% duty cycle for the multiplied clock. Finally, interphase timing distortion may occur when the multiphase clocks pass through the multiplication-ratio control logic, which in turn can generate pulse, suitable for high-frequency multiplied clock generation with low power and a small area. It can also guarantee a 50% duty cycle for its multiplied clock. However, because the output pulses of the pulse generator are generated consecutively [i.e., the kth pulse is generated directly following the (k−1)th pulse], the pulses might overlap owing to process variation or layout mismatch as they pass through the multiplication-ratio control logic; this could cause a short-circuit current to flow in the edge combiner, which in turn could lead to excessive power consumption or malfunction of the frequency multiplier. In addition, the output loading of the edge combiner rapidly increases with the multiplication ratio.

3. PROPOSED SYSTEM

To enhance the lock time, which is an important design parameter in the clock generator, a dual-edge-triggered phase-detector-based DLL core is adopted. Similar to pre- vious frequency multipliers, the proposed frequency multiplier is also composed of a pulse generator, a multiplication-ratio control logic, and an edge combiner. ratio control signal. Finally, the high-speed and highly reliable edge combiner (HSHR-EC) generates one multiplied clock (CLKMUL) using all the outputs of the multiplication- ratio control logic. Since the number of multiphase is 32, the maximum multiplication ratio is 16. HSHR-EC. As the number of signals merged in the precombining stage (NPRE) increases, the number of PU-Ps and PD-Ns required in the push–pull stage are reduced by a factor of NPRE. It might appear that, by increasing NPRE, the maximum multiplied clock frequency of the HSHR-EC can be enhanced; however, because the logic depth and the number of NAND and NOR gates in the precombing stage are equal to log2NPRE and 32(1–1/NPRE), respectively, a large NPRE causes the

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precombining stage to be vulnerable to process variation, which in turn could cause a large deterministic jitter. Thus, NPRE is limited to two, which

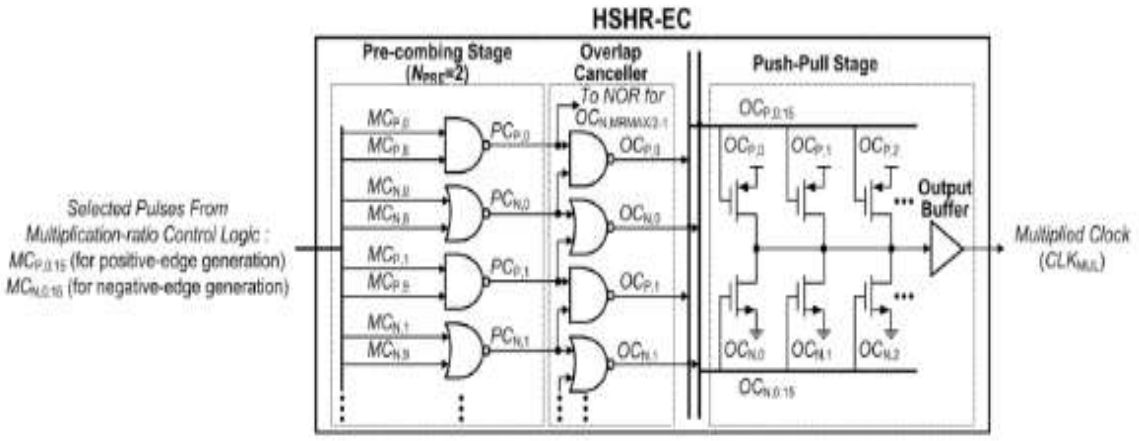

Fig.2. Proposed Structure

corresponds to a logic depth of one in the HSHR-EC, and thus, the precombining stage can be simply realized using NAND and NOR gates.

4. RESULT ANALYSIS

The maximum multiplied clock frequency of the proposed frequency multiplier is compared with the previous frequency multipliers. Because it is determined by the edge-combiner structure, he normalized channel widths of the PU-P and the output buffer with respect to the channel width of the PD-N, fMUL,MAX is the maximum multiplied clock frequency, and ERRDUTY is the duty-cycle error of the multiplied clock. However, because the precombining stage in the HSHR-EC merges two signals into one, the self-loading of the push–pull stage (output loading of the push–pull stage except the loading induced by the output buffer) is halved. The frequency multiplier in has the best performance among the previous

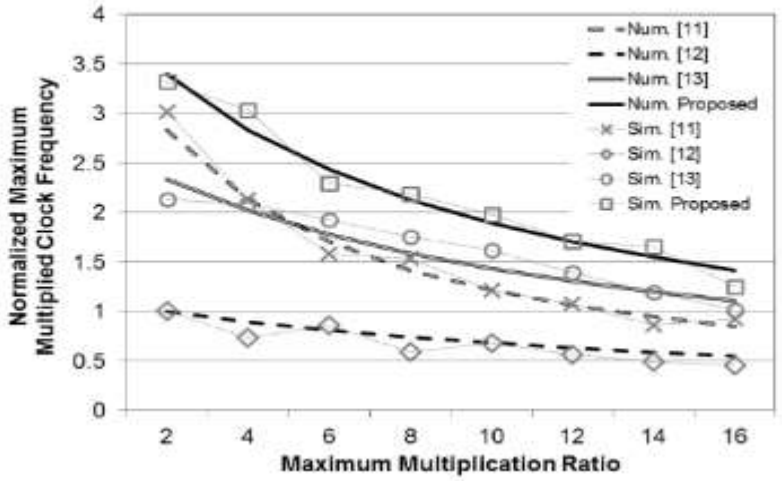

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Fig.3. Numerical analysis and simulation results

frequency multipliers, because the modified DCVSL stage in its edge combiner has better features than that of the edge combinersrequire a high operating frequency. Thus, the proposed clock generator (frequency multiplier with DLL core) achieves the lowest power consumption to frequency ratio among the DLL with frequency multiplier architectures. Because the proposed clock generator has the highest maximum multiplication ratio and the areas of the DLL core and the frequency multiplier are proportional to the maximum multiplication ratio, the area of the proposed clock generator is larger than that of previous DLL

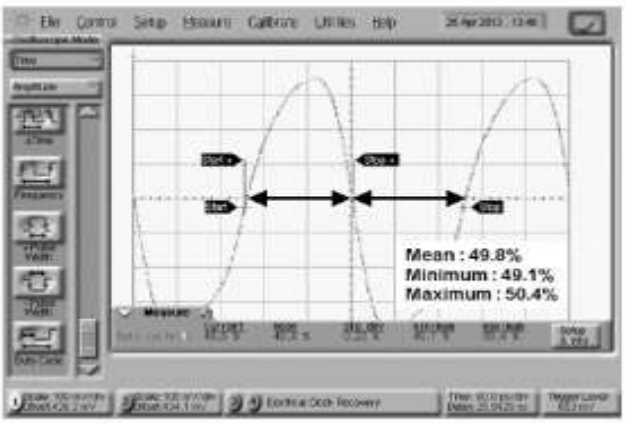

Fig.4. Measured waveform of the multiplied clock

with frequency multiplier architectures. However, the normalized area of the proposed clock generator, which is the area divided by the product of the square of the process technology and the maximum multiplication ratio, is lower than that of other clock generators. where MRMAX is the maximum multiplication factor. Compared with DLL with frequency multiplier architectures, the proposed clock generator shows the superior performance according to both FoM1 and FoM2, as expected. Note that both the multiplying DLL and the PLL architecture in [18] show superior performance than the proposed clock generator in FoM1. Even the area and the multiplication ratio are consid- ered using FoM2, the multiplying DLL in is still shows better performance than the proposed clock generator. This result is mainly due to the outstanding power consumption of the multiplying DLL and the PLL architecture.

CONCLUSION

In this paper, a frequency multiplier for a DLL-based clock generator is proposed. The proposed HSHC-EC guarantees high-speed operation owing to its hierarchical edge-combiner structure and highly reliable operation owing to its use of an overlap canceller. The optimized pulse generator and the multiplication-ratio control logic are proposed to reduce the delay difference between positive and negative edge generation paths. Finally, a numerical analysis is performed to validate its performance.

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