INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2437 - 2441
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

Design Of Arthematic Logic Unit using GDI adder and multiplexer

[1]M.Vishala, [2]Maddana,

[1]PG Scholar, Dept of VLSI System Design, Geetanjali college of engineering & technology,
[2]HOD Dept of ECE, Geetanjali college of engineering & technology.

Abstract:

Power dissipation has a major impact while we are designing any circuit. Since this factor plays a major role in deciding the efficiency of the designed circuit i.e. why in this paper we are proposing a plan for sequential circuits so that we can reduce the power dissipation. Power dissipation which in turn reduces the whole power dissipation of CPU. In this paper, we proposed a low power 1-bit full adder (FA) with 10-transistors and this is used in the design ALU. The proposed design consists of GDI adder based and mux circuits. By using low power 1-bit full adder in the implementation of ALU, the power and area are greatly reduced to more than 50% compared to conventional design and 30% compared to transmission gates. So, the design is attributed as an area efficient and low power ALU .In this, ALU consists of 4x1 multiplexer, 2x1 multiplexer and full adder designed to implements logic operations, such as AND, OR, etc. and arithmetic operations, as ADD and SUBTRACT. GDI cells are used in the design of multiplexers and full adder which are then associated to realize ALU. The simulation results is done T- Spice tool with TSMC018 technologies.

Keywords: Full Adder, ALU, T-Spice.

1. INTRODUCTION

ALU is one of the main components of microprocessor. They use fast dynamic logic circuits and have carefully optimized structures. Its power consumption accounts for a significant portion of total power consumption of data path [1]. ALU also contribute to one of the highest power-density locations on the processor, as it is clocked at the highest speed and is kept busy most of the time resulting in thermal hotspots and sharp temperature gradients within the execution core. Power dissipation is basically the power which is converted to heat and then conducted or radiated away from the device. Electronic and electric devices can have a limit on the current they can safely handle that is not an electronic limit, but a physical one. For instance, a transistor may otherwise be able to handle a certain amount of current, but it is given a lower current rating because the die gets too hot. Dissipation is usually measured in watts, and uses the usual Ohm's law calculations for power. Most of the Very Large Scale IC (VLSI) applications, Full adder circuit is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs. Almost every complex computational circuit requires full adder circuitry. The entire computational block power consumption can be reduced by implementing low power techniques on full adder circuitry. In this paper, from different existed base papers several full adder circuits based on different low power techniques have been proposed targeting.

2. RELATED WORK

Multiplexer will acts as a digital switch. Selection line plays a major role to select particular input. If the number of input lines is „2n‟ and selection lines will be „n‟ selection lines. With the „n‟ selection line

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2437 - 2441
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

the particular „2n" input line will be selected. Figure shows the implementation of 2x1 multiplexer shows the layout of 2x1 multiplexer. The number of selection lines for 2x1 multiplexer is one selection line. With respect to the select line the inputs will be selected. In the same way 4x1 multiplexer also designed to execute arithmetic and logic unit. The number of selection lines required for 4x1 multiplexer is two and with respect to the two selection lines the four inputs will be activated.

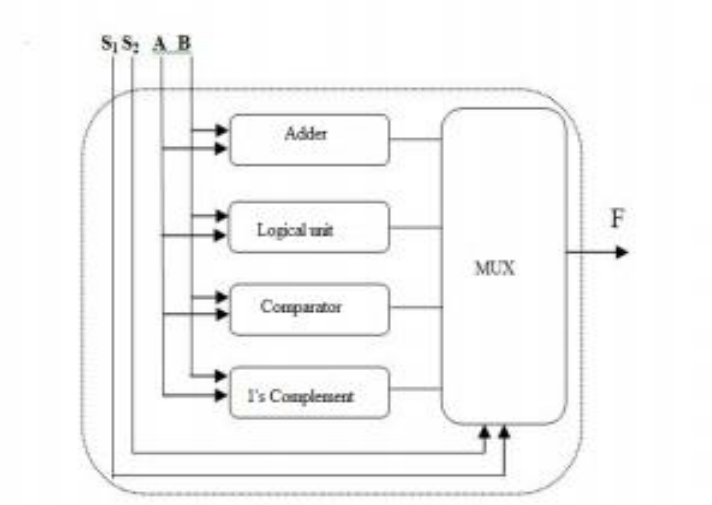

Fig.1. General Structure

One bit full adder circuit is also an important block to design Arithmetic and logic unit. Full adder circuit contains three inputs and two outputs named sum and carry. The operation adds only for one bit numbers. The number of transistors required to design one bit full adder are less so the area will be optimized for the better performance of arithmetic and logic unit circuit design. Recently , the industries are demand for low power, less area and high speed for designing the circuits. With improvement in technology and the enlargement of embedded system used electronic devices such as mobile, laptops, TV applications, power consumption, which is one of the limits in both high & low performance system, has become a primary focus in VLSI digital design. In this paper the adder was based on regular CMOS structure (pull-up and pull-down network) [1].Disadvantage of this paper is but the uses a number of transistors results in high input loads, more power consumption and larger silicon area. Morgenshtein has proposed basic GDI cell [2].By using this GDI cell we design ALU. In digital system design processor is main part of the system. And an ALU is one of the main components of a micro-processor. CPU works as a brain to any system & and ALU works as a brain to CPU.

3. IMPLEMENTATION

The Arithmetic and Logic Unit (ALU) is the critical component in the microprocessor it performs all arithmetic like addition, multiplication, subtraction, etc and logical calculations like OR, XOR, AND, NAND. In computer Central Processing Unit (CPU) is the brain of the computer and ALU is fundamental block of CPU. The processor found inside Graphical Processor Unit is also contains powerful ALU. We design ALU using full adder and the multiplexer circuits as shown in Fig.6. The full adder circuits used here is single bit full adder .the multiplexer circuit is of 4X1 mux and 2X1MUX. The full adder circuits are designed PTLGDI logic style. The multiplexer used in the ALU is for input signal selection and to determine

what kind operation to performed .The multiplexer is implemented using six and two transistors .the transistor count is reduced and power consumption is also low compared to pass transistor multiplexer. This design is simple in terms of time and area consuming.

Fig.2. Design of ALU

The full adder performs the computing functions of ALU. The pass transistor logic reduces the parasitic capacitance and GDI logic increase the speed of the operation. In existing method ALU is designed using 4X1 mux, 2X1 mux and full adder. The multiplexers were designed using pass transistor logic. And the full adder is implemented using 8 transistors. The transistor count is reduced and thus the power.

4. SIMULATION ANALYSIS

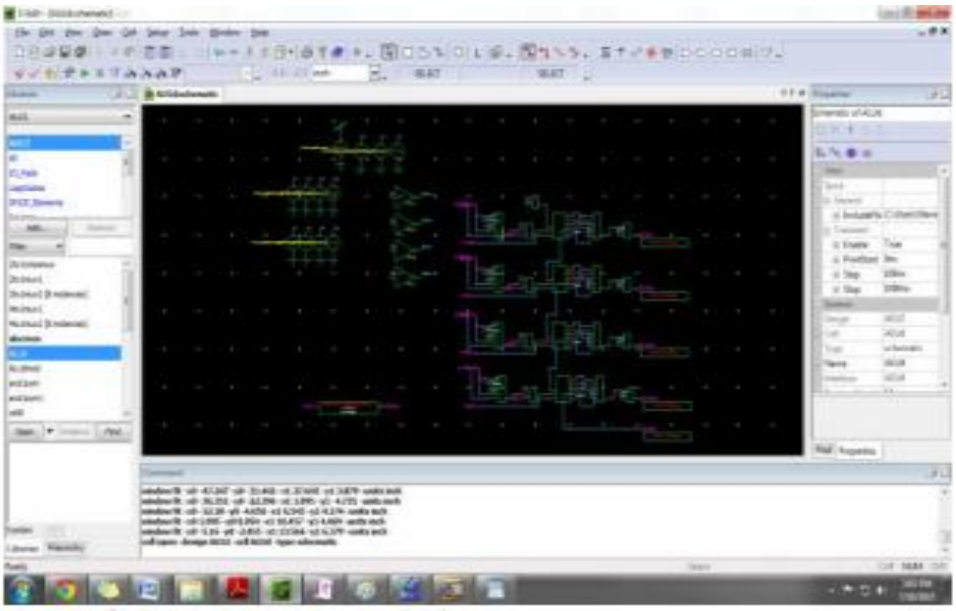

Fig.3.Simulation System

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2437 - 2441
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

ALU design by using proposed GDI technique uses a less number of transistor so area is optimized. if use less no.of transistor then speed is also increase then operating time is reduced. so proposed GDI ALU uses a low power and less no.of transistor, design complexity. figure 9 shows the number of transistor are used for designing ALU and internal blocks, in that GDI technique uses a less number of transistors.

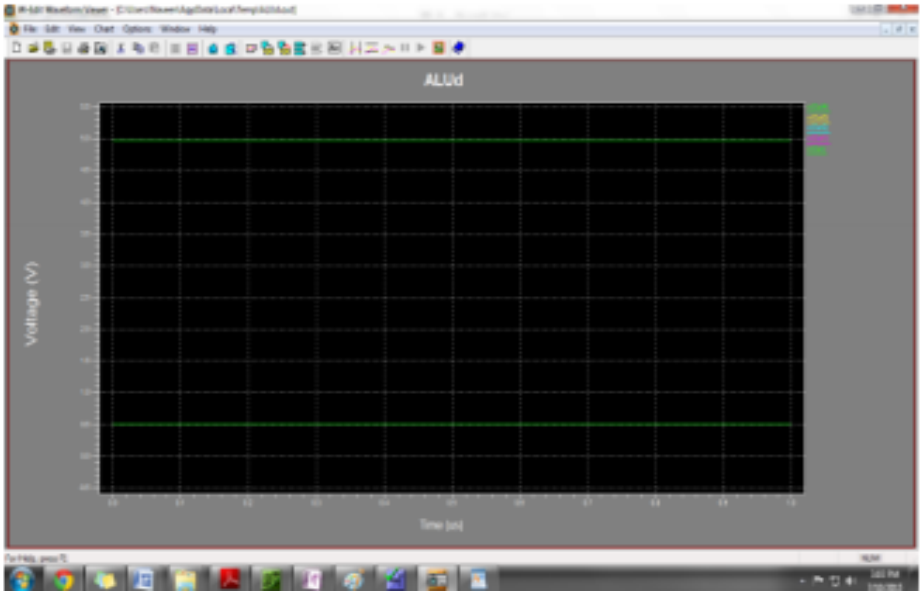

Fig.4.ALU Simulation

A low power and area optimizing technique is introduced and the components with this technique are implemented. Later the comparison between the number of transistor used in CMOS and GDI design of ALU is done. And in the results is shows that this GDI design is reduces the power and the number of transistor and hence optimize the area of ALU as well increase its working speed.

CONCLUSION

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuits static power dissipation is negligible thus not considered as compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by P = CLf VDD2. The power supply is directly related to dynamic power. The numbers of power supply to ground connections are reduced in GDI implementation which reduces the dynamic power consumption. With Using GDI technology designing a ALU consumer Less area, less power consumption.

REFERENCES

[1] J. Han and M. Orshansky, ―Approximate computing: an emerging paradigm for energy-efficient design,‖ in ETS'13, May 2013.
[2] R. Hegde and N.R. Shan hag, ―Soft digital signal processing,‖ IEEE Trans. VLSI Syst., vol. 9, no. 6, pp. 813– 823, 2001.
[3] Vaibhav Gupta, Debabrata Mohapatra, Anand Raghunathan," Low-Power Digital Signal Processing Using Approximate Adders" IEEE Trans. on CAD Of IC and Systems, vol. 32, no. 1, Jan 20

[4] P. Kulkarni, P. Gupta, and M. Ercegovac, ―Trading accuracy for power with an underdesigned multiplier architecture,‖ in Proc. 24th IEEE Int. Conf. VLSI Design, Jan. 2011, pp. 346–351.
[5] V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, ―IMPACT: Imprecise adders for low-power approximate computing,‖ in Proc. IEEE/ACM Int. Symp. Low-Power Electron. Design, Aug. 2011, pp. 409–414.
[6] D. Shin and S. K. Gupta, ―Approximate logic synthesis for error tolerant applications,‖ in Proc. Design, Automat. Test Eur., 2010, pp. 957–960.