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Modelling Of Adders Using CMOS GDI For Vedic Multipliers

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Abstract:

Advancement in the VLSI technology leads to the reduction in chip size and increase in chip density. As the chip density increases the overall power consumption and the complexity also increases. As the performance of any system is measured mainly on power consumption, it is recommended to use low power VLSI Design techniques. In this paper, we would discuss the GDI logic and its application in the modeling of adders for Vedic Multiplier design. Adders are of prime importance, the design of reliable and efficient adder for a VLSI based embedded application matters. This paper primarily deals with the design of Ripple Carry Adder, Kogge Stone Adder, and Brent Kung Adder using CMOS and GDI logic. Urdhava Triyagbhayam sutra is used to design multipliers. Later a comparative analysis based on the simulation results is made.

Keywords: CMOS, Brent kung adder, GDI Logic.

1. INTRODUCTION

The increasing prominence of portable systems demands high chip density along with low power consumption. Now a day's reducing the power consumption has become an important goal in the design of digital integrated circuits. One of the methods to meet this goal is the design improvements at the logic level. Traditional digital circuits were designed using complementary metal oxide semiconductors (CMOS). A new Low power VLSI design technique called GDI (Gate diffusion Input) is used in the design of digital components. This Technique has comparatively more advantages over the traditional CMOS design. This paper gives comparative analysis based on the performance of CMOS and GDI techniques. A Multiplier is the fundamental block of almost all the processors.

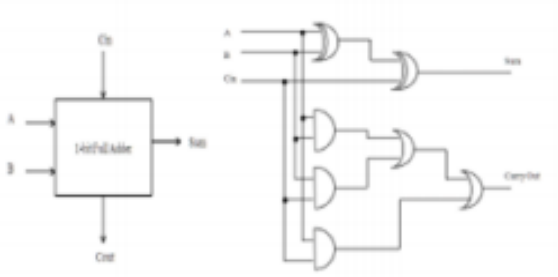

Fig.1. General description

Hence a high-speed and area efficient multiplier is needed. Multiplication operation is performed by the series or parallel addition concepts. Design of adders with GDI technique will improve the performance of multipliers. GDI cell looks similar to the CMOS inverter but the major difference is that the GDI cell has one PMOS and NMOS transistors connected in cascade resulting in three input terminals N, P, G. where N is the input terminal of NMOS, P is input to the PMOS and G is connected to the common gate of NMOS

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and PMOS. These terminals could be given a supply VDD or Grounded or input signal depending on the circuit design. In conventional CMOS inverter circuit, the PMOS and NMOS diffusion inputs are always either VDD or Ground.

2. RELATED WORK

Addition of N bit numbers is performed with the help of N full adders arranged such that the carry output of the full adder is input to the next full adder. This kind of arrangement is called Ripple carry adder. In Ripple Carry Adder the carry is rippled from the one adder to the next full adder. Ripple carry adder is simple to design and takes less time. However, the Ripple carry adder is relatively slow since each full adder must wait for the carry bit from the previous adders. A Full adder performs the addition operation on three-bit binary numbers A, B and C.

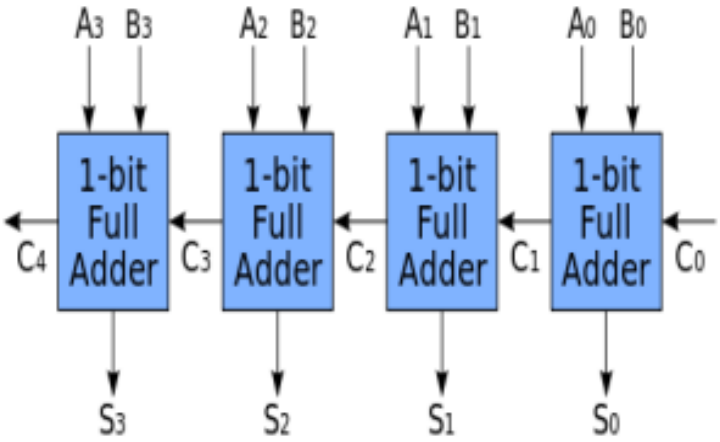

Fig.2. Carry Adder

The output of the full adder is SUM and Carry. It can be implemented using Two XOR gates and One MUX. Ripple carry adder is designed using four full adders which are designed using GDI logic. The gate count of the Ripple carry adders using GDI logic is 40 Transistors and the area is 804.19 µm square which is comparatively very less. The power consumed by the 4 bit RCA is 11.622µW. The Parallel Prefix Adders (PPA) is the family adders derived from Carry look ahead (CLA) adders. Carry Look Ahead adders are designed to overcome the carry propagation delay in RCA. These adders pre compute the generator and propagation bits, these bits are further combined using fundamental carry operation (FCO) denoted by the symbol (o). It is observed that the complexity of the carrier increases with adder bit width, Hence the higher order CLA becomes complex. To overcome the drawback of CLA, Parallel Prefix Adders are designed.

3. IMPLEMENTATION

Multipliers are designed with the help GDI based adders and a Vedic multiplication technique called "Urdhva- Tiryakbhyam, Which can be used not only for decimal multiplication but also for binary multiplication. This mainly consists of the parallel generation of partial products and performing the addition operation simultaneously. This algorithm can be used for N×N bit multiplications. within the block diagram 4x4 there are four 2x2 Vedic multiplier modules, and three RCAs which are of four-bit size are used. The four bit ripple carry adders are used for addition of two four bits, and likewise, totally four are

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used at intermediate stages 3 of the multiplier. The carry generated from the first ripple carry adder passed on to the next ripple carry adder and there are two zero inputs for second ripple carry adder.

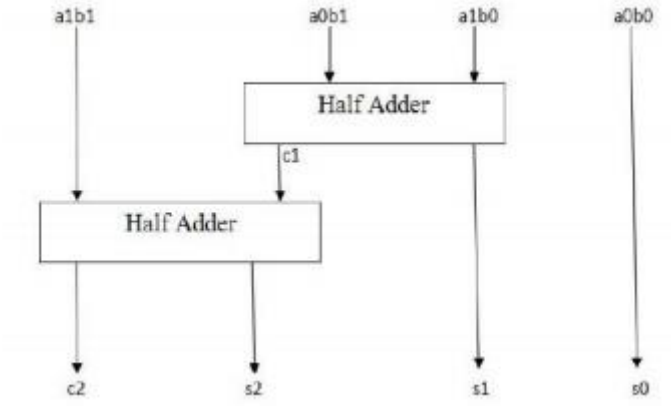

Fig.3. Verdic multiplier

The arrangement of the RCAs is shown in below block diagram which can reduce the computational time such that the delay can be decreased. After performing all the steps the result (Sn) and Carry (Cn) is obtained and in the same way at each step the previous stage carry is forwarded to the next stage, and the process goes on. To illustrate this technique, let us consider two decimal numbers 252 and 846 and the multiplication of two decimal numbers 252×846 is explained by using the line diagram. First multiply the both numbers present on the two sides of the line and then first digit is stored as the first digit of the result and remaining digit is stored as pre carry for the next coming step and the process goes on and when there is more than one line then calculate the product of end digits of first line and add the result to the product obtained from the other line and finally store it as a result and carry. The obtained carry can be used a carry for the further steps and finally we will get the required result which is the final product of two decimal numbers 252x846. Take the initial carry value as the zero. For clear understanding purpose we explained the complete algorithm in the below line diagram such that each bit represents a circle and number of bits equal to the number of circles present.

4. ANALYSIS

Within the block diagram 4x4 totally there are four 2x2 Vedic multiplier modules, and three ripple carry adders which are of four bit size are used. The four bit ripple carry adders are used for addition of two four bits and likewise totally four are use at intermediate stages 3 of multiplier. The carry generated from the first ripple carry adder is passed on to the next ripple carry adder and there are two zero inputs for second ripple carry adder. The arrangement of the ripple carry adders are shown in below block diagram which can reduces the computational time such that the delay can be decrease. To explain this method let us consider 2 numbers with 2 bits each and the numbers are A and B where A=a0a1 and B=b0b1 as shown in the below line diagram. First the least significant bit (LSB) bit of final product (vertical) is obtained by taking the product of two least significant bit (LSB) bits of A and B is a0b0. Second step is to take the products in a crosswise manner such as the least significant bit (LSB) of the first number A (multiplicand) is multiplied with the next higher bit of the multiplicand B in a crosswise manner. The output generated is 1- Carry bit and 1bit used in the result as shown below. Next step is to take product of 2 most significant bits (MSB)

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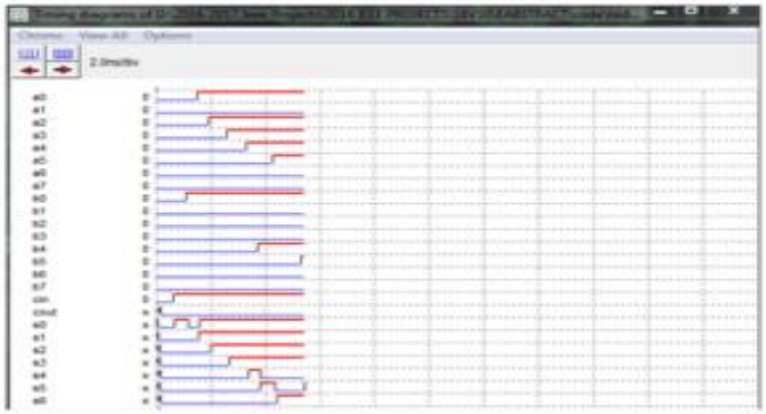

Fig.4.Waveform output

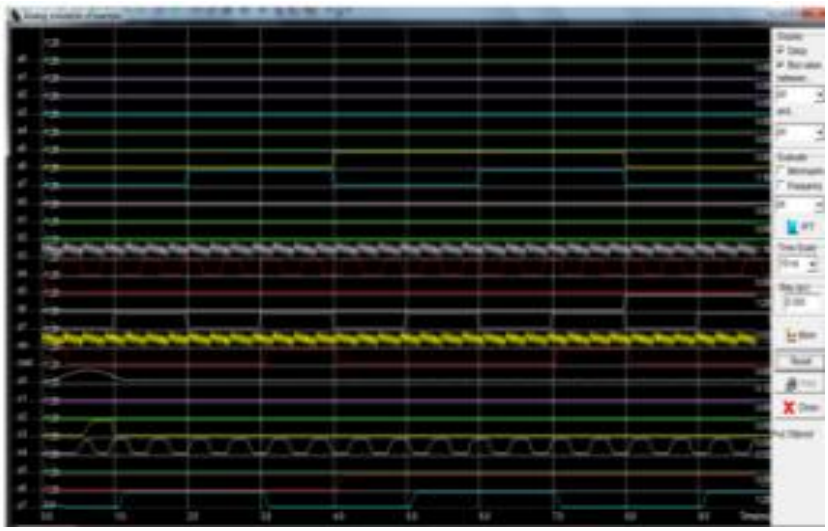

Fig.5.Analysis

and for the obtained result previously obtained carry should be added. The result obtained is used as the fourth bit of the final result and final carry is the other bit.

CONCLUSION

Adders are core and an essential block in many modules which involve computation and play a vital role in the design of multipliers. Hence the design and implementation of the adders are a prime concern. In this paper adders (RCA, KSA, BKA) based on GDI logic are used in Vedic Multiplier design. A comparative result is obtained. From the results, it is clear that the adders designed using GDI design style has less transistor count, occupy minimum area and power when compared to CMOS design style.

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