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# HIGH STEP-DOWN CONVERSION BUCK CONVERTER WITH LOW SWITCH VOLTAGE STRESS MONITORING

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**Abstract**

This paper present a non-isolated interleaved buck converter, constituted by two switches, two diodes, two voltage balance capacitors, and three inductors. It is similar to a three level buck converter, but the two switches interleaved to share the converter power between the two interleaved modules. The interleaving technique reduce the voltage stress across the switch approximately equal to half the input voltage and peak current through the switch to half of the load current. So the converter is suitable for high power applications. Also it has low switching losses and used for high frequency applications. Higher frequency converters have reduced component size. The in front voltage balance capacitors helps in automatically balancing the inductor current. So it requires no complex current control methods. Simulation of the new interleaved buck converter is done with 200V Dc input, 240W output power, and 50 KHz frequency.

***KeyWords*:** Interleaved Buck Converter (IBC), duty- cycle (D), Voltage stress, Automatic uniform current sharing….

## 1. INTRODUCTION

An interleaved buck converter (IBC) is widely used as a non-isolated, step-down, high-output-current, and low output current ripple converter with simple control and structure. Interleaving technique connects dc-dc converters in parallel to share the power flow between two or more conversion chains it implies a reduction in the size, weight and volume of inductors and capacitors. The proposed converter has conversion ratio approximately half of conventional IBC for small duty cycles, smaller the D better the bucking. In conventional IBC use of small D to achieve better conversion ratio have disadvantages like, increased- losses, peak current of switch, and increased inputcurrent ripple so size of input filter also increases. The simple control chips produce a PWM signal with little mismatch in D compared to other interleaved module, due to difference in driver and power switches. To solve the above mentioned problems of un-balanced current-sharing, the capacitive voltage division is introduced by two separate input capacitors; the main objectives of the new voltage-divider circuit in the converter are both dividing the input voltage for reducing voltage stresses of active switches and also for

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increasing the step-down conversion ratio. As a result, the converter possesses the low switch voltage stress characteristic. Moreover, due to the charge balance of the capacitor, the converter features automatic uniform current sharing characteristic of the interleaved phases without adding extra complex control circuitry. Also since the two input switches are operating in continuous conduction mode by automatic uniform current sharing characteristic, the input current to the switches are also continuous.

The proposed converter can be used for high power applications like, distributed power systems**,** battery storage systems**,** VRMs (Variable Regulator Modules) of CPU board**,** battery chargers**,** fuel cell battery storage, led drivers etc. Conventional IBC in high input voltage or high power applications have disadvantages like, voltage stress of switch equal to input voltage so high voltage rated devices are used. High-voltage rated elements suffers from high on-state resistance which means high switching losses. Also high output capacitor is used, so the size and cost of the converter are increased. The proposed converter has voltage stress equal to half of input voltage due to presence of input voltage divider. The proposed IBC i designed for high switching frequency and high power applications. Higher switching frequency implies reduced component size and cost of the converter.

## 1. PROPOSED CONVERTER

The proposed converter is similar to a three- level buck converter, but the two input capacitors are not connected to each other, and also, there is an auxiliary inductor at the converter output stage. The two active switches are controlled by two PWM pulses 180◦ out of phase. The operation and the key waveforms of the proposed converter for $D < 0.5$ and D > 0.5 are explained.

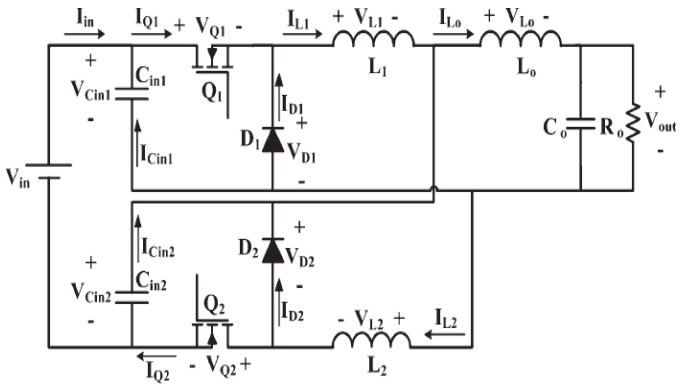


**Fig-1:** Circuit Diagram of Proposed IBC

## 2. MODES OF OPERATION- D<0.5

### Mode 1

During this mode switch Q1 and D2 are turned on, while Q2 and D1 are turned off. The charge on Cin1 is discharging and IL1 is increasing. Inductor L2 is releasing its energy to Lo. Cin2 is charging from input voltage. Also get the KVL for three loops.

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**Mode 2**

During this mode switch $Q_1$ and $Q_2$ are turned off, while $D_1$ and $D_2$ are turned on. The inductors $L_1$ and $L_2$ are releasing its energy to load $L_o$. Input capacitors $C_{in1}$ and $C_{in2}$ are charging through separate paths. Get the KVL for four loops.

**Mode 3**

During this mode switch $Q_2$ and $D_1$ are turned on, while $Q_1$ and $D_2$ are turned off. The charge on $C_{in2}$ is discharging and $I_{L2}$ is increasing. Inductor $L_1$ is releasing its energy to $L_o$. $C_{in1}$ is charging from input voltage. Get the KVL for three loops.

**Mode 4**

Mode 4 operation is same as mode 2. In this mode the two switches are turned off and there are four conduction paths. It includes two discharging paths of inductor $L_1$ and $L_2$ and two charging paths of input capacitors $C_1$ and $C_2$. Therefore the KVL equations are same as Mode 2.

## 3. MODES OF OPERATION- D>0.5

The mode 1 and mode 3 of opertaion for D<0.5 and D>0.5 are same.

**Mode 2 and 4**

In these modes switches $Q_1$ and $Q_2$ are turned on and diodes $D_1$ and $D_2$ are turned off. Both the input capacitors are discharging its charge to Lo via $L_1$ and $L_2$. Output inductors are also charging from input voltage.

## 4. DESIGN

**Gain Derivation**

Considering equation the equation for $V_{Lo}(t)$ for one switching period is zero, that is the volt-second balance (VSB) equation for $L_o$ in one switching period, $V_{Lo}$ is given as:

$V_{Lo}(t) = 0.$ (1)

The voltage-second balance equation for L1 is obtained as follows,

$V_{L1ON} * T_{ON} + V_{L1OFF} * T_{OFF} = 0$ (2)

Substitute for above equation from KVL equations, we get;

$(V_{Cin1} - V_{out})DT = V_{out}(1 - D)T$ (3) Similarly for $L_2$, the voltage-second balance equation for $L_2$ is obtained as;

$(V_{Cin2} - V_{out})DT = V_{out} * (1 - D)T$ (4) Gain of the proposed converter can be obtained as follows:

$$\frac{Vout}{Vin} = \frac{D}{2-D} \quad (5)$$

Moreover, $V_{Cin}$ is

$$V_{cin} = \frac{Vin}{2-D} \quad (6)$$

The components are designed based on the assumption that Capacitors $C_{in1}$, $C_{in2}$, and $C_o$ is large enough so that their voltage variations can be ignored. Also the currents in $L_1$ and $L_2$ are constant. Circuit is designed considering $C_{in1}=C_{in2}$ and $L_1=L_2$.

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$$= \frac{\frac{VoTs(1-D)}{\Delta IL}}{\frac{IoD(1-2D)T}{(2-D)\Delta Vcin}}$$

$L_1 = L_2 =$

$C_{in1} = C_{in2}$

$$Co = \frac{\Delta IL}{8(\Delta Vo - \Delta IL * ESR)fs}$$

**Voltage Stress**

From mode 1, when $D_1$ is off voltage across diode1 is $V_{cin1} = Vcin = \frac{Vin}{2-D}$

When $Q_2$ is off, voltage across switch 2 is, $V_{cin2}$

$$V_{cin2} = Vcin = \frac{Vin}{2-D}$$

From mode 3, when $D_2$ is off voltage across diode2 is, $V_{cin2}$

$$V_{cin2} = Vcin = \frac{Vin}{2-D}$$

When $Q_1$ is off voltage across switch 1 is, $V_{cin1}$

$$V_{cin1} = Vcin = \frac{Vin}{2-D}$$

## 5. SIMULATION RESULTS- D<0.5

For simulating the above buck converter choose the following values. I had assumed that $\Delta IL$ = 20% $Io$ and $\Delta VO_{UT}$ = 20% $VO_{UT}$ and $\Delta IO$=40%IO. Based on the above equation capacitor and inductor values are calculated using the parameters given in table.

**Table-1:** Simulation Parameters

| S.I No | Parameters Used | Specification |
|---|---|---|
| 1 | Power | 240W |
| 2 | Input voltage | 200Volt |
| 2 | Output voltage | 24Volt |
| 3 | Output current | 10A |
| 4 | Frequency | 50Khz |
| 5 | Capacitor($C_{in1}$ &$C_{2in2}$) | 11µF |
| 5 | Inductors(L1&L2) | 192µH |
| 6 | Output inductor | 96 µH |

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| | | |
|---|---|---|
| 7 | Output capacitor | 2 µF |
| 8 | R load | 2.4Ω |

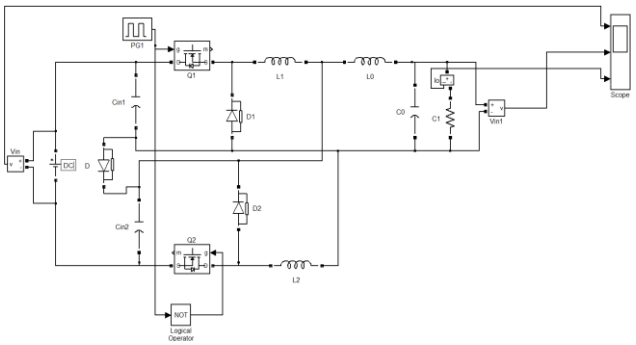

**Fig-2:** Simulation Diagram

Based on chosen values of input the component values and output is calculated theoretically using the equations obtained from steady state analysis.

**Output Voltage**

Output voltage is obtained by multiplying gain of the converter with input voltage, So calculated and simulated result are given below, Gain $= \frac{Vout}{Vin} = \frac{D}{2-D} = 0.12$

Output voltage = 0 .112*200 = 24V

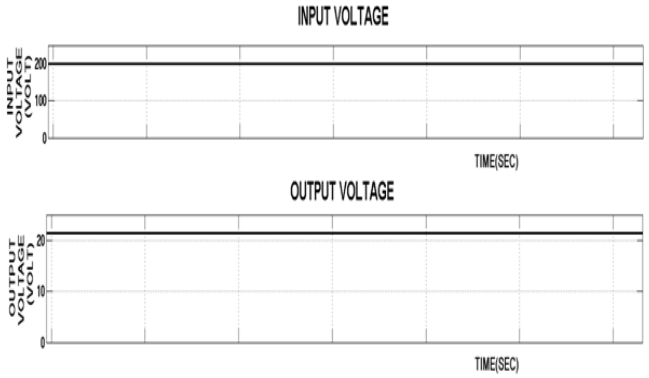


**Fig-3:** Input and Output Voltages

Input and output current waveforms are given below, Output current $= \frac{Po}{Vo} = 10A$

Input current = 1.2A

 

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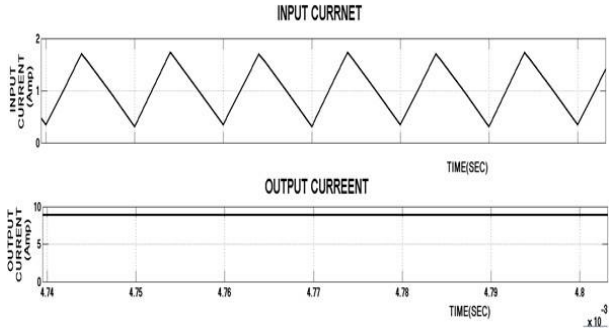



**Fig-4:** Input and Output Currents

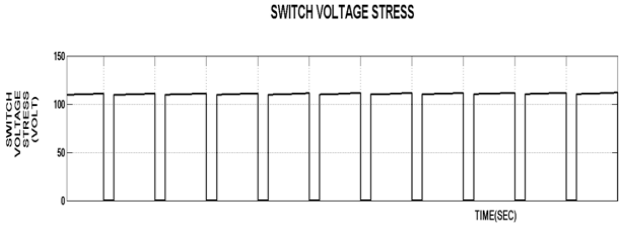
**Voltage Stress**

The voltage stress of switch and diode are obtained as:

Switch voltage stress = diode voltage stress =

= 110

$$Vcin = \frac{Vin}{2-D}$$



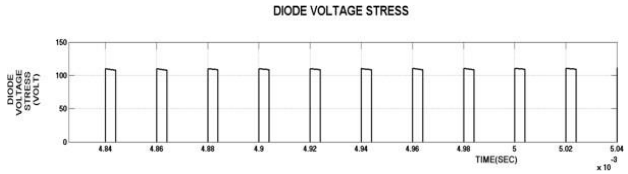




**Fig-5:** Voltage Stress

**Current Stress**

The current stress of switch and diode are obtained from following equations:

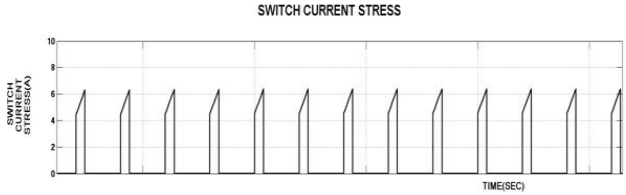
Peak current stress of switches

$= \frac{Vo(1-D)T}{2.L} + \frac{Io}{2-D} = 6.5A$

Average current stress of diodes

= = 5.58A

$$Vs = \frac{Io}{2-D}$$



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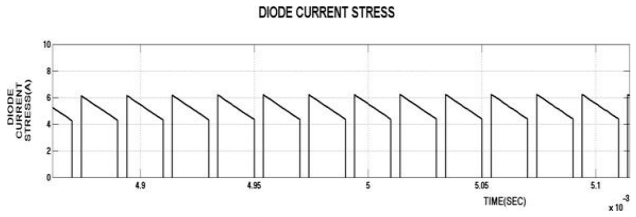


**Fig-6:** Current Stress

## 6. SIMULATION RESULTS- D>0.5

For simulating the above buck converter choose the following values. I had assumed that $\Delta IL$ = 20% $Io$ and $\Delta VO$UT = 20% $VO$UT and ΔIO=40%IO. Based on the above equation capacitor and inductor values are calculated using the parameters given in table.

**Table-2:** Simulation Parameters

| S.I No | Parameters Used | Specification |
|---|---|---|
| 1 | Power | 240W |
| 2 | Input voltage | 200Volt |
| 2 | Output voltage | 85Volt |
| 3 | Output current | 2.8A |
| 4 | Frequency | 50Khz |
| 5 | Capacitor($C_{in1}$ &$C_{2in2}$) | 3.3µF |
| 5 | Inductors($L_1$&$L_2$) | 0.34mH |
| 6 | Output inductor | 48 µH |
| 7 | Output capacitor | 0.16 µF |
| 8 | R load | 30Ω |

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**Output Voltage**

Output voltage is obtained by multiplying gain of the converter with input voltage, So calculated and simulated result are given below, Gain = $\frac{Vout}{Vin} = \frac{D}{2-D}$ = 0.428

Output voltage = 0 .428*200 = 85V


**Fig-7:** Input and Output Voltages

Input and output current waveforms are given below, Output current = $\frac{Po}{Vo}$ = 2.8A

Input current = 1.19A

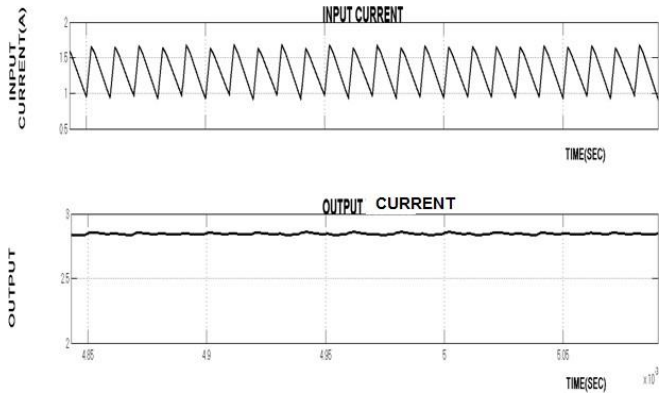
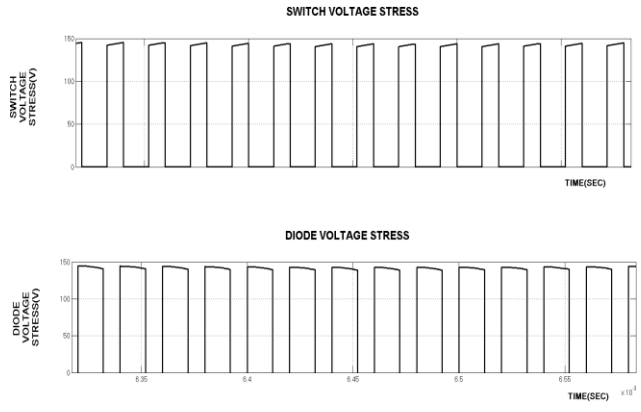



**Fig-8:** Input and Output Currents

**Voltage Stress**

The voltage stress of switch and diode are obtained as: Switch voltage stress = diode voltage stress = $Vcin = \frac{Vin}{2-D}$ = 142V



## CONCLUSION

In the discussed converter input voltage is divided into two thus the voltage stresses of active switches are reduced to half the input voltage and also increased the step-down conversion ratio. As a result, the converter possesses the low switch voltage stress characteristic. Moreover, due to the voltage balance capacitor, the converter features automatic uniform current sharing characteristic of the interleaved phases without adding extra complex control circuitry. Also since the two input switches are operating in continuous conduction mode by automatic uniform current sharing characteristic, the input current to the switches are also continuous.The future scope and applications of paper are high power applications, distributed power systems**,** battery storage systems**,** VRMs of CPU board**,** battery chargers, fuel cell battery storage, led driver etc.Recommended modifications for the circuit are increasing the number if interleaving to increase step down conversion and also introducing an efficient rectifier in front for applications like power supply for electronics equipments.

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